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<b>Form PTO-1449 Modified</b>		Docket No. <b>D5116-00002A</b>	Serial No. Technology Center 2800, 109-2678427
List of Patent and Publications Cited by Applicant (Use several sheets if necessary)		Applicant <b>Saxena et al.</b>	APR 11 2001 Technology Center 2800, 109-2678427
U. S. Department of Commerce Patent and Trademark Office		Filing Date <b>09/29/2000</b>	Group <b>2812</b>

**U. S. PATENT DOCUMENTS**

Examiner Initial	Cite No.	Document No.	Date	Name	Class	Subclass
mrh	AA	4,795,964	1/3/89	Mahant-Shetti et al.	324	60
mrh	AB	4,939,681	7/3/90	Yokomizo et al.	364	578
mrh	AC	5,067,101	11/19/91	Kunikiyo et al.	364	578
mrh	AD	5,068,547	11/26/91	Gascoyne	307	443
mrh	AE	5,070,469	12/3/91	Kunikyo et al.	364	578
mrh	AF	5,286,656	2/15/94	Keown et al.	324	158
mrh	AG	5,301,118	4/5/94	Heck et al.	364	468
mrh	AH	5,438,527	8/1/95	Feldbaumer et al.	364	578
mrh	AI	5,486,786	1/23/96	Lee	327	378
mrh	AJ	5,502,643	3/26/96	Fujinaga	354	488
mrh	AK	5,625,268	4/29/97	Miyanari	318	696
mrh	AL	5,627,083	5/6/97	Tounai	438	18
mrh	AM	5,629,877	5/13/97	Tamegaya	364	578
mrh	AN	5,655,110	8/5/97	Krivokapic et al.	395	500
mrh	AO	5,703,381	12/30/97	Iwasa et al.	257	48
mrh	AP	5,778,202	7/7/98	Kuroishi et al.	395	306
mrh	AQ	5,790,479	8/4/98	Conn	368	118
mrh	AR	5,798,649	8/25/98	Smayling et al.	324	551
mrh	AS	5,867,033	2/2/99	Sporck et al.	324	763
mrh	AT	5,903,012	5/11/99	Boerstler	257	48
mrh	AU	5,966,527	10/12/99	Krivokapic et al.	395	500.35

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Form PTO-1449 Modified				Docket No. D5116-00002A	RECEIVED APR 11 2001 TC 2100 MAIL ROOM	Serial No. 09/675,427
List of Patent and Publications Cited by Applicant (See several sheets if necessary)				Applicant Saxena et al.	RECEIVED APR 2 2001 TECHNOLOGY CENTER 2100	
U. S. Department of Commerce Patent and Trademark Office				Filing Date 09/29/2000	Group 2812	
U. S. PATENT DOCUMENTS						
Examiner Initial	Cite No.	Document No.	Date	Name	Class	Subclass
mrh	AV	5,982,929	11/9/99	Ilan et al.	382	200
mrh	AW	6,005,829	12/21/99	Conn	368	118
mrh	AX	6,063,132	5/16/00	DeCamp et al.	716	5
mrh	AY	6,066,179	5/23/00	Allan	716	4
mrh	AZ	6,072,804	6/6/00	Beyers, Jr.	370	450
mrh	BA	6,075,417	6/13/00	Cheek et al.	331	44
mrh	BB	6,075,418	6/13/00	Kingsley et al.	331	57
mrh	BC	6,118,137	9/12/00	Fulford, Jr. et al.	257	48
mrh	BD	6,124,143	9/26/00	Sugasawara	438	18
mrh	BE	6,134,191	10/17/00	Alfke	368	118
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<b>Form PTO-1449 Modified</b>		Docket No. <b>D5116-00002A</b>	Serial No. <b>09/675,427</b>
List of Patent and Publications Cited by Applicant (Use several sheets if necessary)		Applicant <b>Saxena et al.</b>	
U.S. Department of Commerce Patent and Trademark Office		Filing Date <b>09/29/2000</b>	Group <b>2812</b>
Examiner Initial <i>MRH</i>	Cite No.	<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)</b>	
	BF	WALTON et al., "A Novel Approach for Reducing the Area Occupied by Contact Pads on Process Control Chips", <i>Proc IEEE 1990 Int. Conference on Microelectronic Test Structures</i> , Vol. 9, March 1990, pgs. 75-80	
	BG	BECKERS AND HILLTROP, "The Spidermask: A New Approach for Yield Monitoring Using Product Adaptable Test Structures", <i>Proc IEEE 1990 Int. Conference on Microelectronic Test Structures</i> , Vol. 8, March 1990, pgs. 61-66	
	BH	LIEBMAN et al. "Understanding Across Chip Line Width Variation: The First Step Toward Optical Proximity Correction", SPIE Vol. 3051, pgs.124-136.	
	BI	PCT International Search Report, March 13, 2001	
	BJ	CONTI. M. et al., Parametric Yield Formulation of MOS IC's Affected by Mismatch Effect. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , May 1999, Vol. 18, No. 5, Pages 582-596	
	BK	TO. H. et al., Mismatch Modeling and Characterization of Bipolar Transistors for Statistical CAD. <i>IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications</i> , July 1996, Vol. 43, No. 7, Pages 608-610	
	BL	FELT. E. et al., Measurement and Modeling of MOS Transistor Current Mismatch in Analog IC's, 1994 <i>IEEE/ACM International Conference on Computer-Aided Design</i> , November 1994, Pages 272-277	
	BM	MICHAEL. C. et al., A flexible Statistical Model for CAD of Submicrometer Analog CMOS Integrated Circuits, 1993, <i>IEEE/ACM International Conference on Computer-Aided Design</i> , November 1993, Pages 330-333	
	BN	OGRENCI. A. et al., Incorporating MOS Transistor Mismatches Into Training of Analog Neural Networks, <i>Proceedings of NC, International ICSC/IFAC Symposium on Neural Computation</i> , September 1998, Abstract only	
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